ABSTRACT

A processor surrogate (320/520) is adapted for use in a processing node (S1) of a multiprocessor data processing system (300/500) having a plurality of processing nodes (P0, S1) coupled together and to a plurality of input/output devices (330, 340, 350/530, 540, 550, 560) using corresponding communication links. The processor surrogate (320/520) includes a first port (372, 374/620, 622) comprising a first set of integrated circuit terminals adapted to be coupled to a first external communication link (370/590) for coupling (P0) of the plurality of processing nodes (310, 320/510, 520), a second port (382, 384/630, 632) comprising a second set of integrated circuit terminals adapted to be coupled to a second external communication link (380/592) for coupling to one (350/550) of the plurality of input/output devices (330, 340, 350/530, 540, 550, 560), and an interconnection circuit (390, 392/608, 612, 614) coupled between the first port (372, 374/620, 622) and the second port (382, 384/630, 632).